FIG. 1

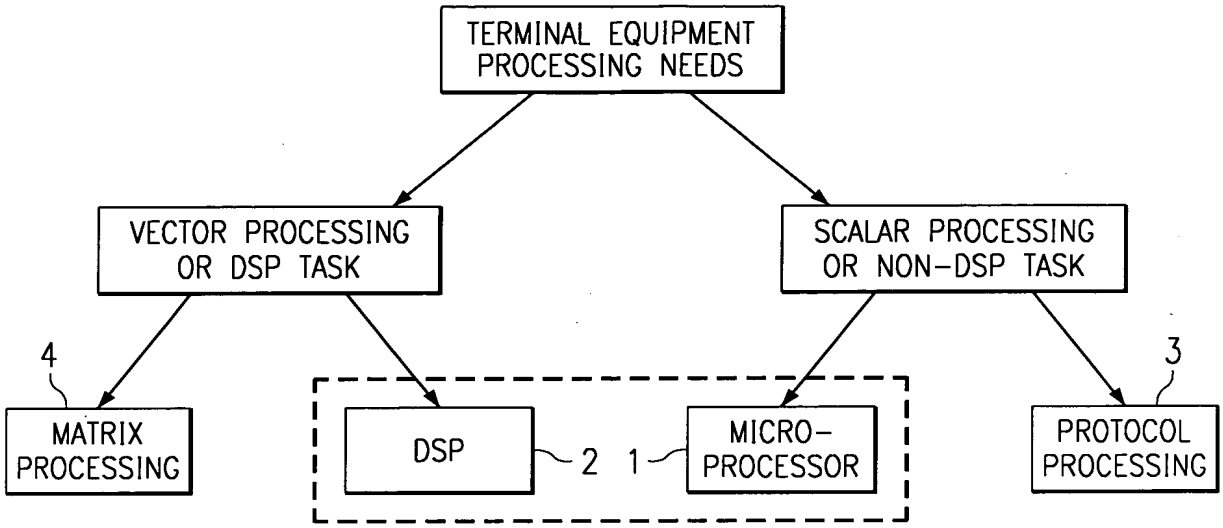


FIG. 2

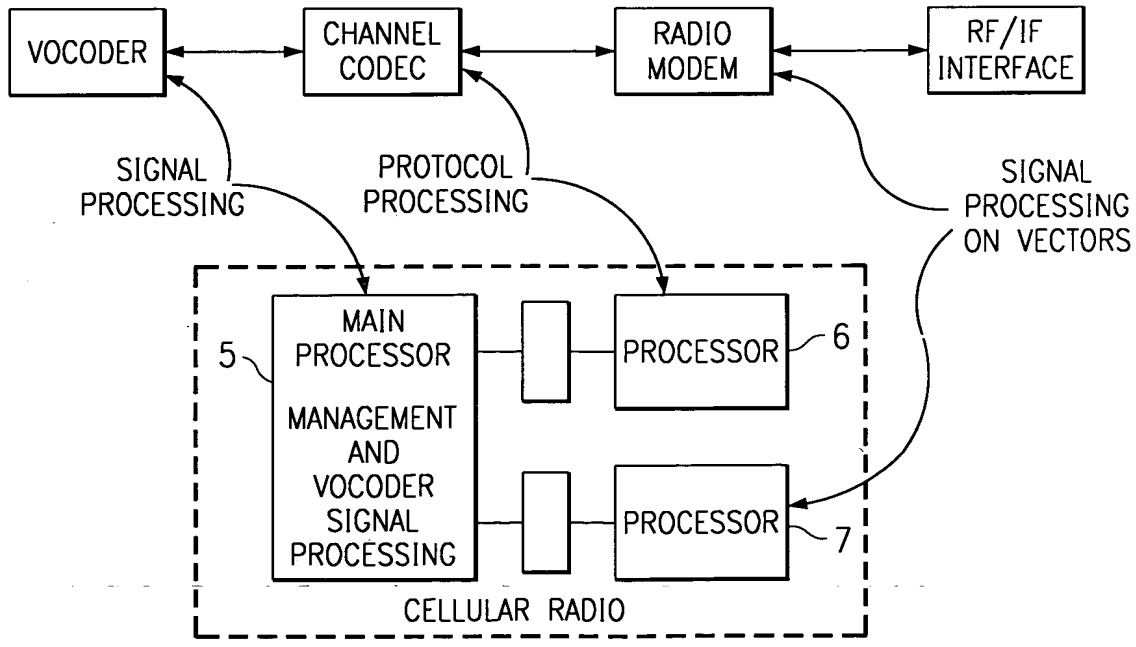


FIG. 3

PERFORMANCE OF CHANNEL CODEC ROUTINES

ROUTINES	DSP UTILIZATION C5x	PROC PROTOCOL PP UTILIZATION
16 BIT CRC	6 INSTR/BIT	4 INSTR/BIT
IDENTIFICATION	5 INSTR/BIT	1 INSTR/BIT

RATIO		
SEL/INSTR EFFICIENCY	x1	x2.2
NO. OF TRANS	58 KTx	6.5 KTx
MIPS	28 MIPS	28x2.2=62 MIPS DSP

FIG. 4

PERFORMANCE OF MODEM ROUTINES

ROUTINES	DSP UTILIZATION C5x	ARRAY PROC
METRIC COMPUTATION 57 SYMBOLS (4 SAMPLES)	43800 CYCLES	4400 CYCLES

RATIO		
INSTRUCTION SETTING EFFICIENCY	x1	x10
MIPS	28 MIPS	28x10=280 MIPS DSP

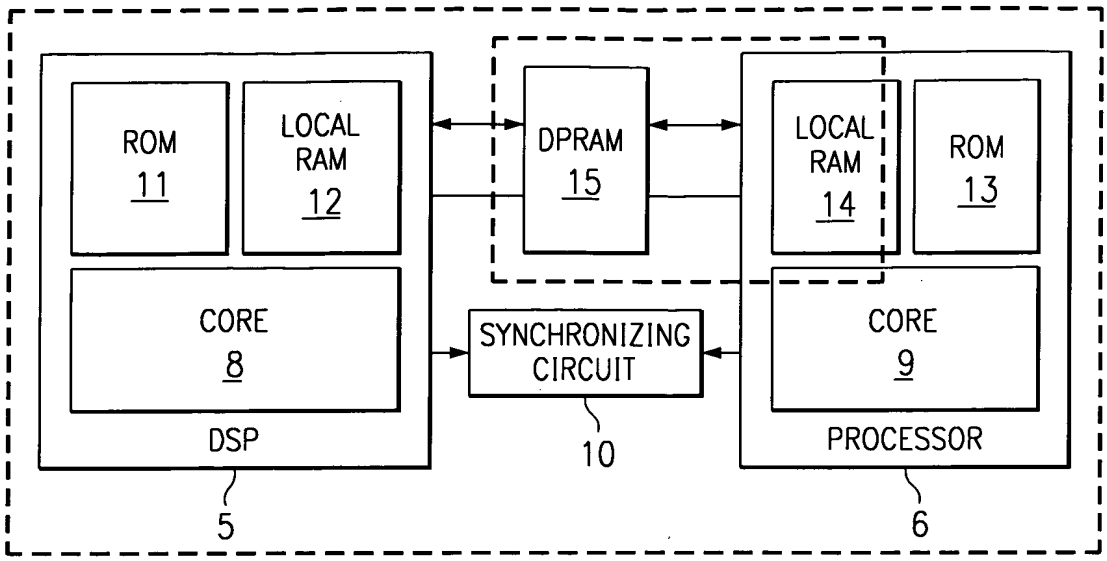


FIG. 5

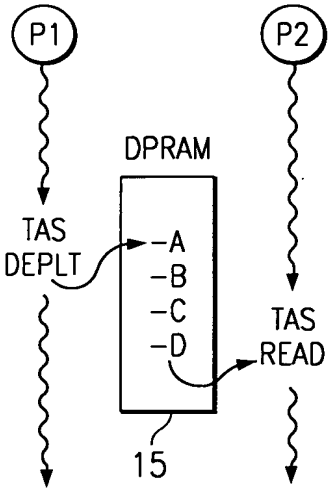


FIG. 6

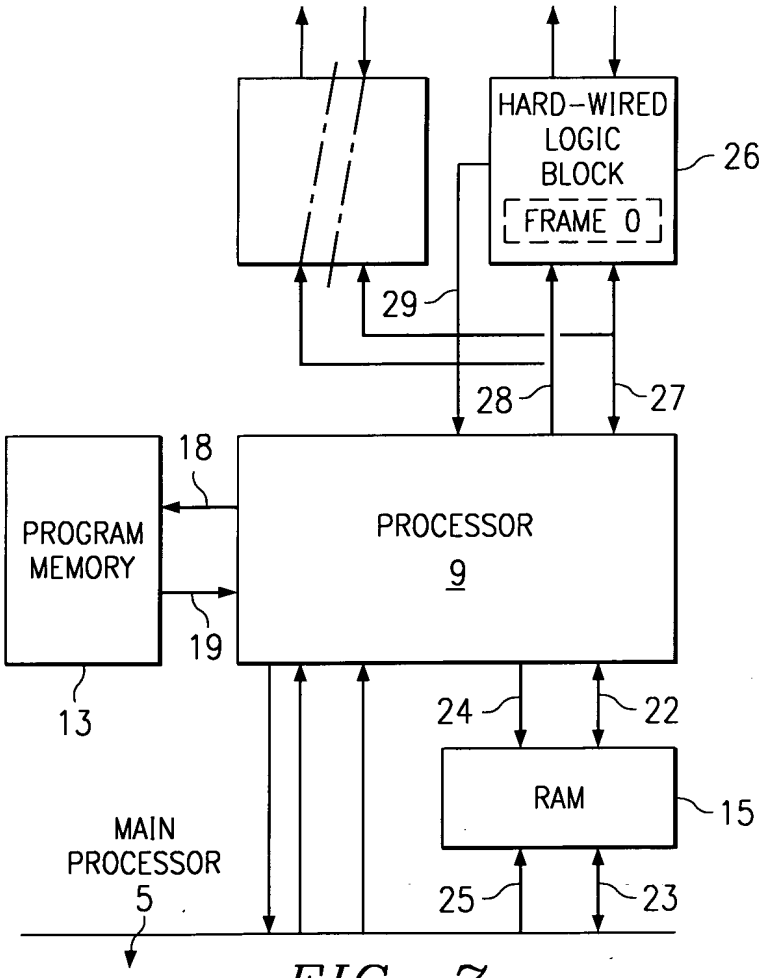


FIG. 7

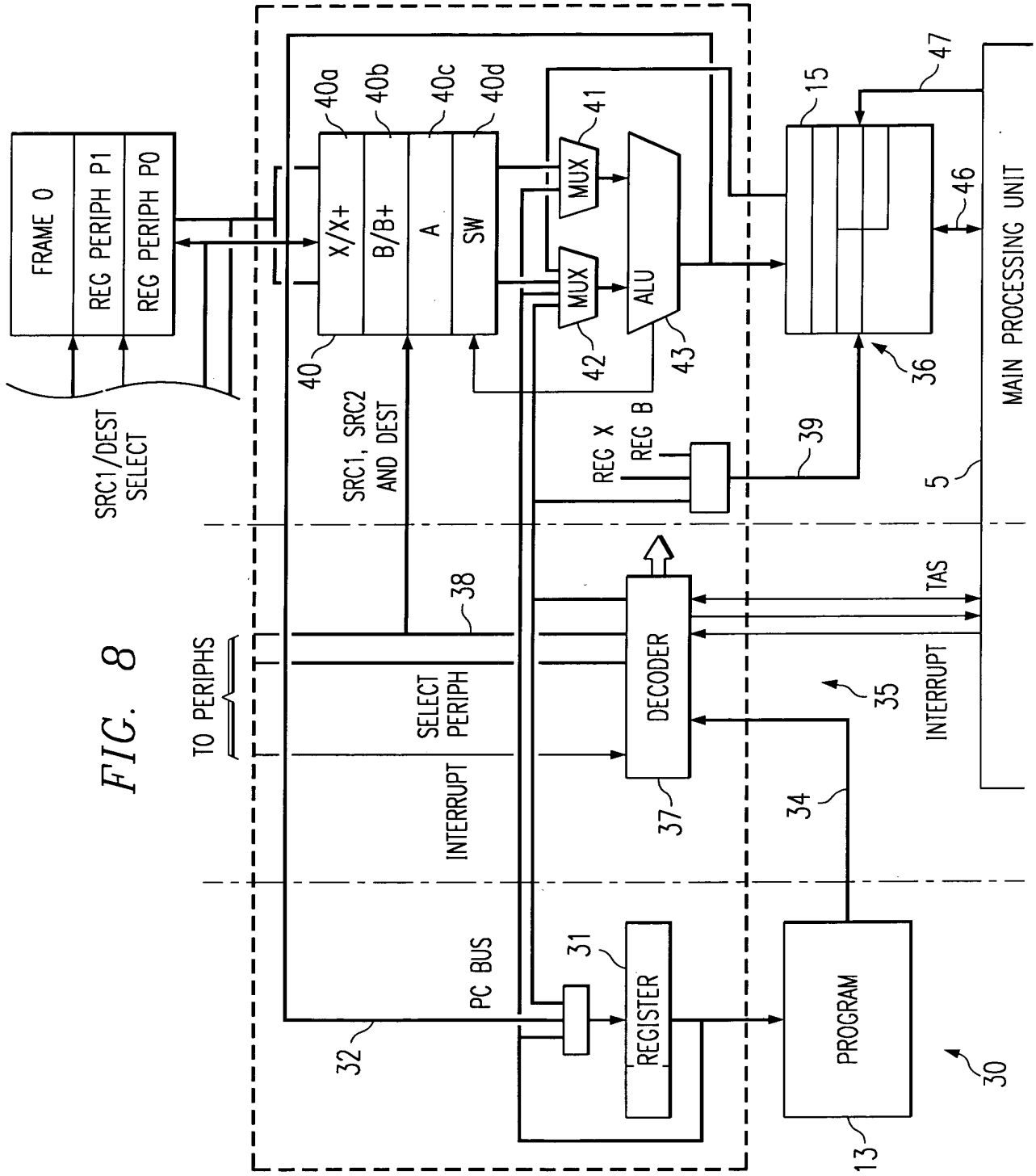

FRAME 0
REG PERIPH P1
REG PERIPH P0
SRC1/DEST SELECT
40a
40b
40c
40d
X/X+
B/B+
A
SW
40
SRC1, SRC2 AND DEST
MUX
MUX
41
42
ALU
43
REG X
REG B
39
15
47
46
36
MAIN PROCESSING UNIT
5
TAS
INTERRUPT
35
DECODER
37
34
38
TO PERIPHS
SELECT PERIPH
INTERRUPT
PC BUS
31
REGISTER
32
PROGRAM
13
30

FIG. 8

FIG. 9

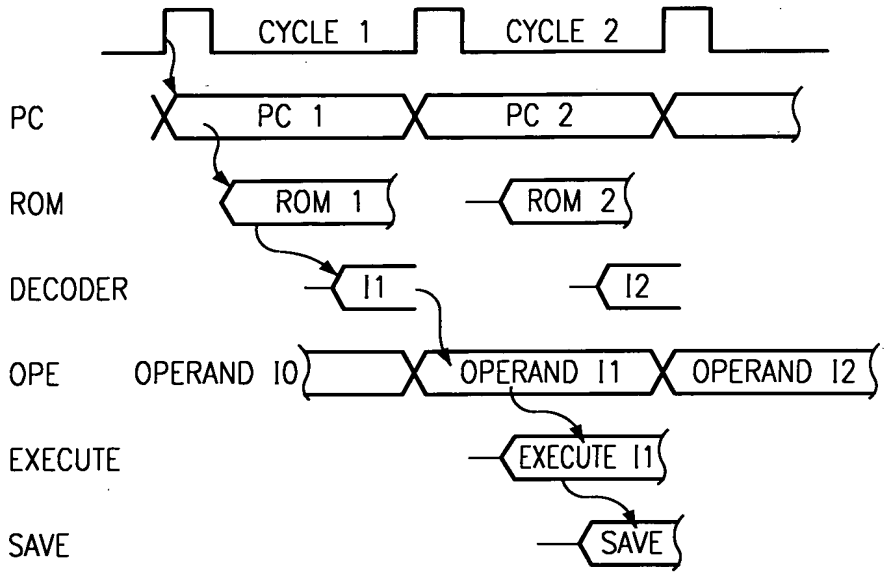


FIG. 11

TYPE	OP CODE												
0	0 0	ALU	Cc	1	K		W	Rm	K				INTEGER/ TRANSFER
1	0 1	ALU	Cc	1	DMA		W	Rm	DMA			L	
2	1 0	ALU	Cc	1	@	+	W	Rm	Rn	FP	S	L	
3	1 1	CODE	Cc		@	D	W	PMA					MONITORING
4	1 1	CODE	Cc		@	+	W		Rn				

FIG. 10

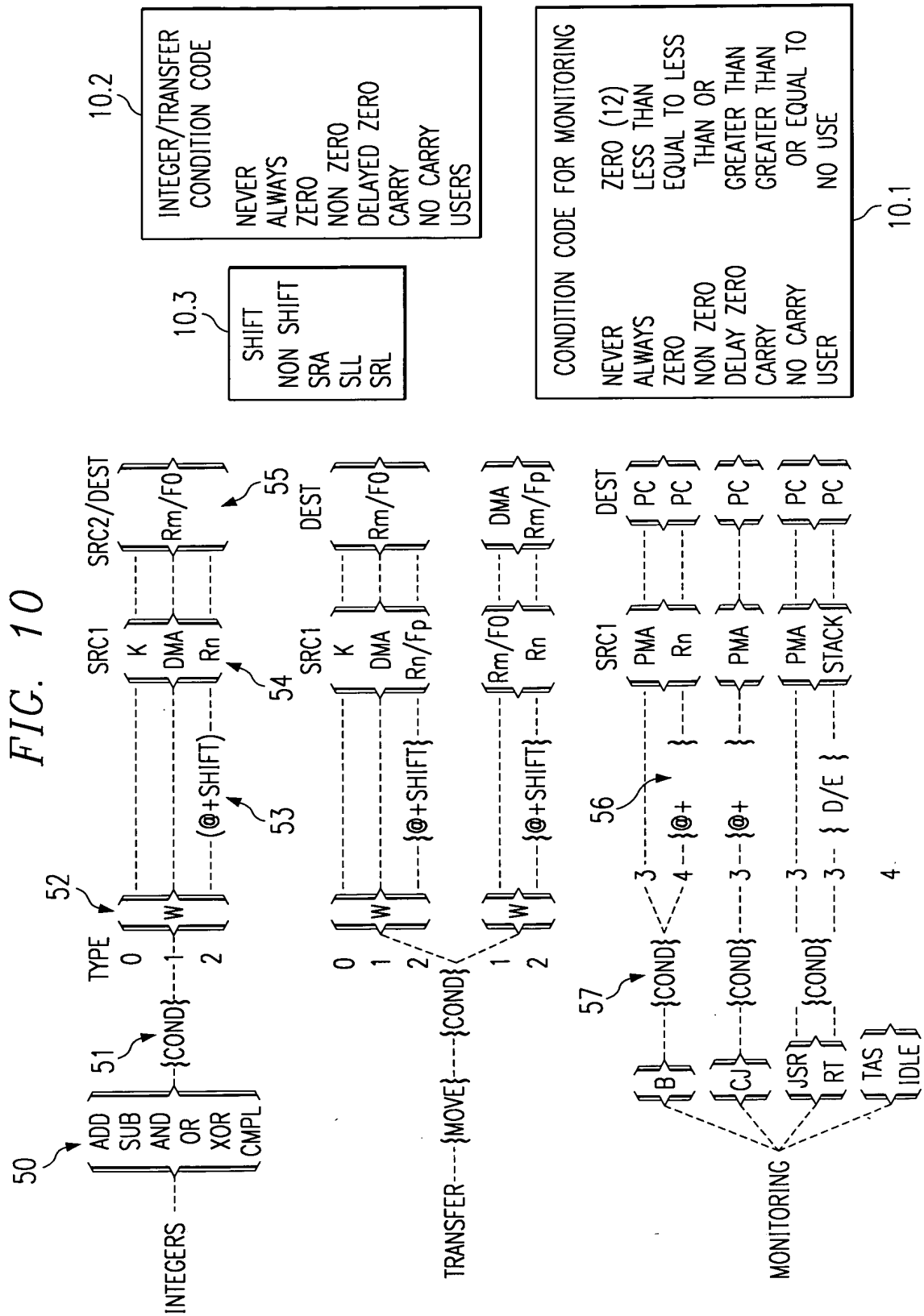

10.2
INTEGER/TRANSFER
CONDITION CODE
NEVER
ALWAYS
ZERO
NON ZERO
DELAYED ZERO
CARRY
NO CARRY
USERS
10.3
SHIFT
NON SHIFT
SRA
SLL
SRL
CONDITION CODE FOR MONITORING
NEVER
ALWAYS
ZERO
NON ZERO
DELAY ZERO
CARRY
NO CARRY
USER
ZERO (12)
LESS THAN
EQUAL TO LESS
THAN OR
GREATER THAN
GREATER THAN
OR EQUAL TO
NO USE
10.1
50
51
52
53
54
55
56
57
INTEGERS
ADD
SUB
AND
OR
XOR
CMPL
{COND}
TYPE
SRC1
SRC2/DEST
K
DMA
Rn
Rm/F0
(@+SHIFT)
TRANSFER
{MOVE}
DEST
Rn/Fp
DMA
Rm/Fp
MONITORING
PMA
PC
B
CJ
JSR
RT
TAS
IDLE
STACK
D/E
{@+
W

FIG. 12

ALU
0 - SUB
1 - CPL
2 - ADD
3 - AND
4 - OR
5 - XOR
6 - PASSA
7 - SUBC

CODE
0 - ST TYPE 1
1 - ST TYPE 2
2 - B TYPE 3
3 - B TYPE 4
4 - CALL
5 - RTS
6 - RTI
7 - STOP

Cc	
0 - NEVER	8 - Z12
1 - ALWAYS	9 - LO
2 - Z	10 - LE
3 - NZ	11 - G
4 - ZD	12 - GE
5 - C	13 - NU
6 - NC	14 - (BL)
7 - USER	15 -

Rm/Rn
0 - P0
1 - P1
2 - A
3 - B
4 - X
5 - PC
6 - SW
7 - SP

W
0 - R/W BYTE
1 - R/W WORD

--->

L
0 - Rm LOW
1 - Rm HIGH

L
0 - DMA/Rn LOW
1 - DMA/Rn HIGH

S
0 - PASS
1 - SRA
2 - SLL
3 - SRL

FIG. 14

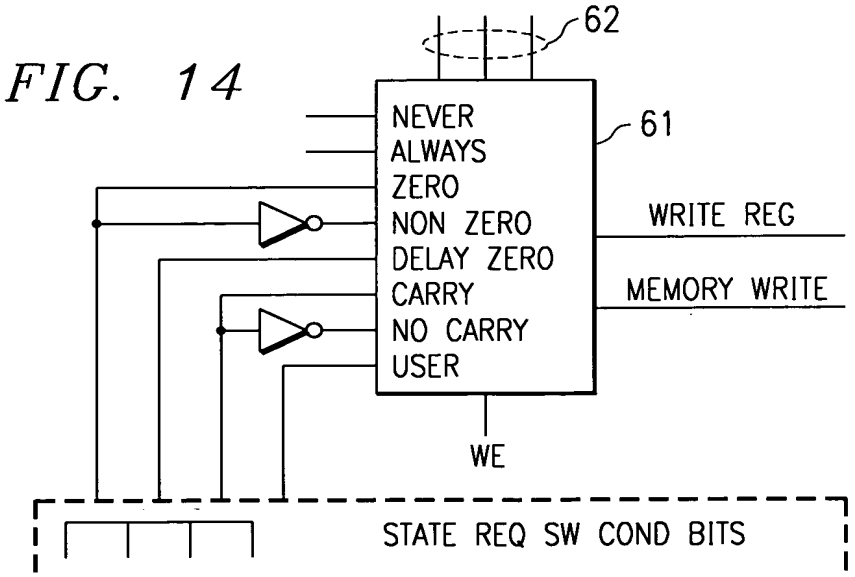
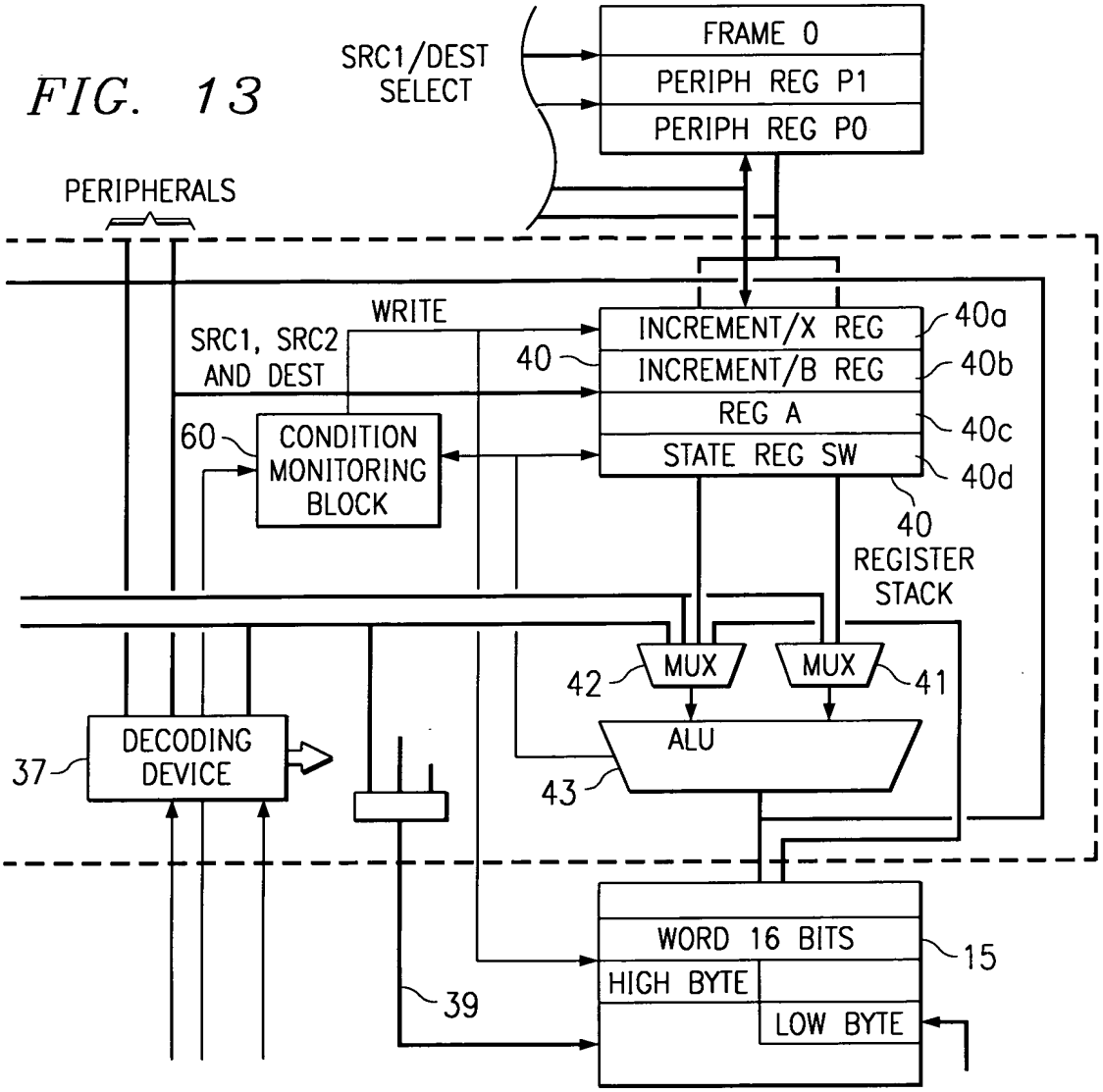


FIG. 13


SRC1/DEST SELECT
FRAME 0
PERIPH REG P1
PERIPH REG P0
PERIPHERALS
WRITE
SRC1, SRC2 AND DEST
40
INCREMENT/X REG
INCREMENT/B REG
REG A
STATE REG SW
40a
40b
40c
40d
60
CONDITION MONITORING BLOCK
40 REGISTER STACK
MUX
MUX
42
41
ALU
43
37
DECODING DEVICE
WORD 16 BITS
HIGH BYTE
LOW BYTE
15
39

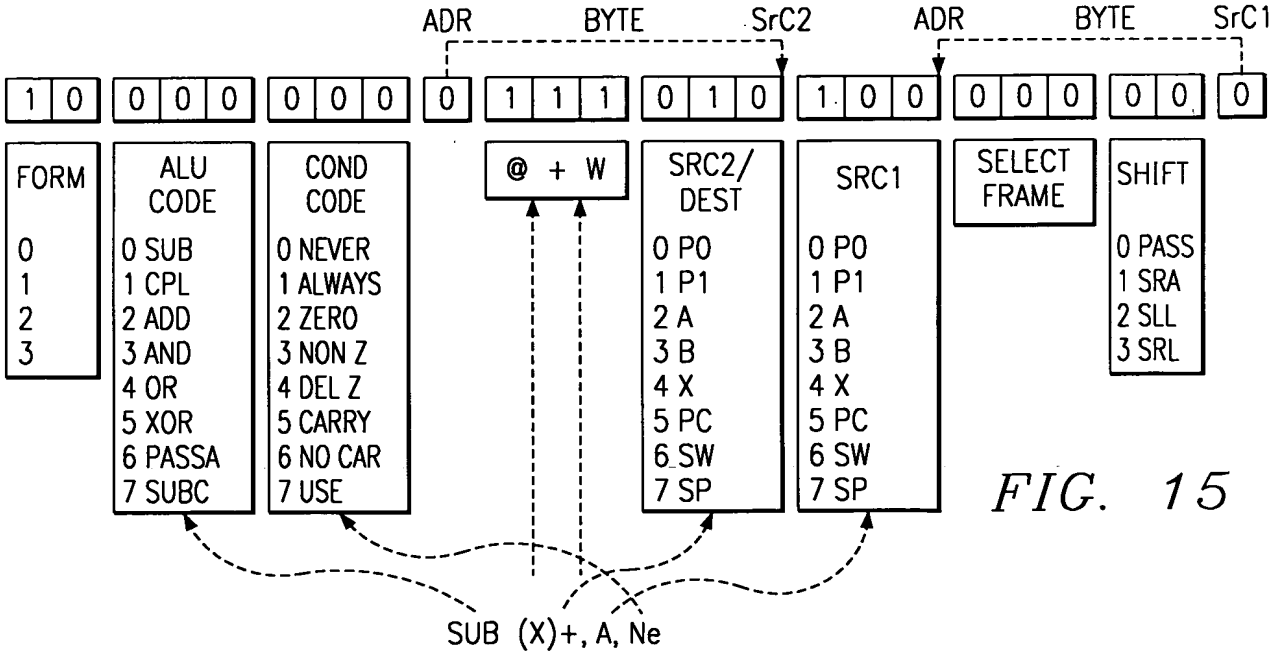

ADR
BYTE
SrC2
ADR
BYTE
SrC1
1 0
0 0 0
0 0 0
0
1 1 1
0 1 0
1 0 0
0 0 0
0 0
0
FORM
0
1
2
3
ALU CODE
0 SUB
1 CPL
2 ADD
3 AND
4 OR
5 XOR
6 PASSA
7 SUBC
COND CODE
0 NEVER
1 ALWAYS
2 ZERO
3 NON Z
4 DEL Z
5 CARRY
6 NO CAR
7 USE
@ + W
SRC2/ DEST
0 P0
1 P1
2 A
3 B
4 X
5 PC
6 SW
7 SP
SRC1
0 P0
1 P1
2 A
3 B
4 X
5 PC
6 SW
7 SP
SELECT FRAME
SHIFT
0 PASS
1 SRA
2 SLL
3 SRL
SUB (X)+, A, Ne

FIG. 15

FIG. 16

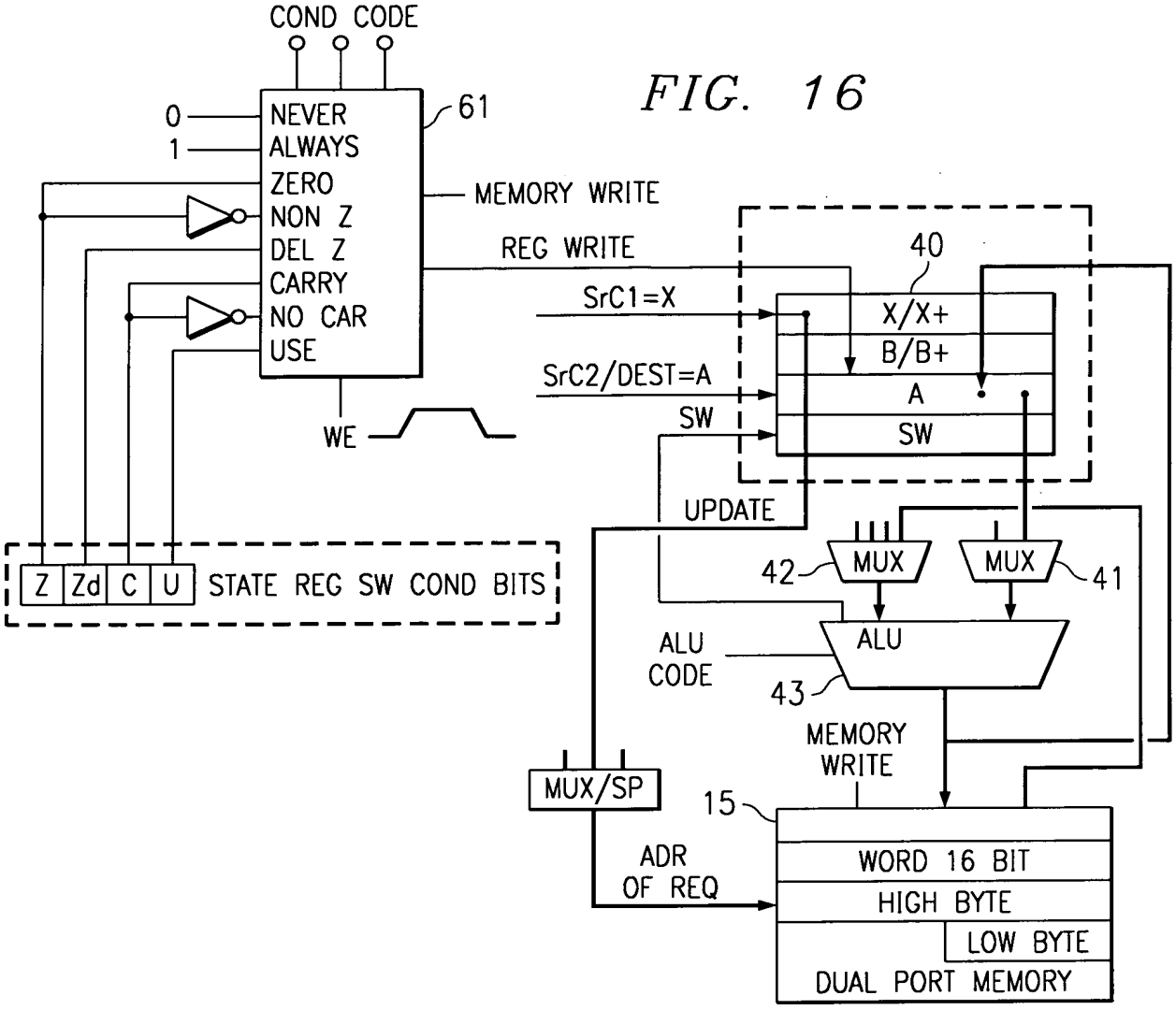
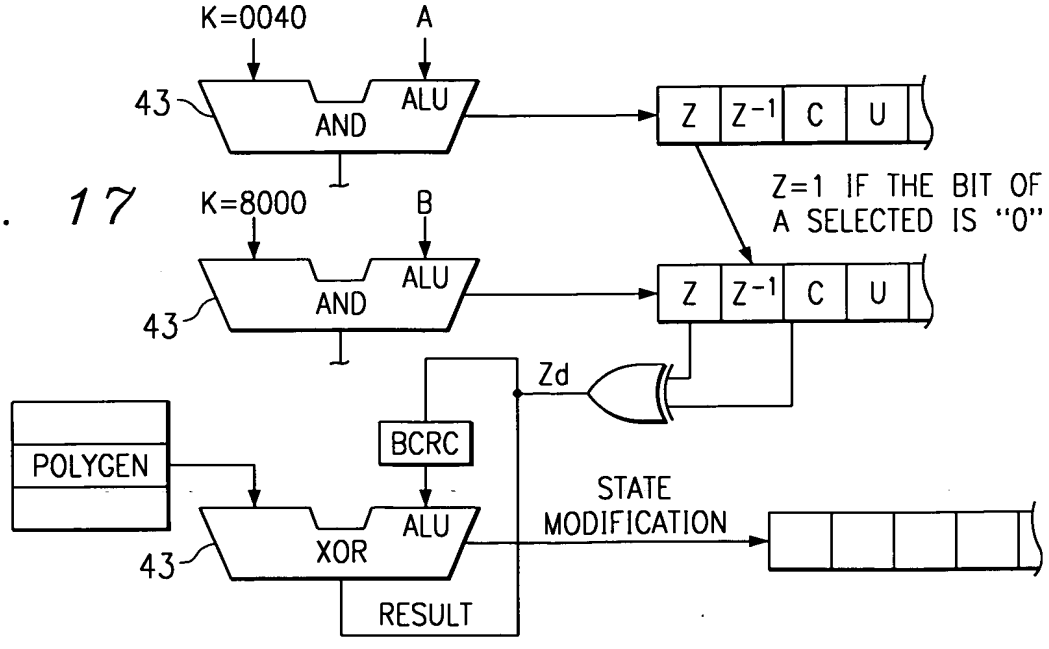

COND CODE
0
1
NEVER
ALWAYS
ZERO
NON Z
DEL Z
CARRY
NO CAR
USE
61
MEMORY WRITE
REG WRITE
WE
40
SrC1=X
SrC2/DEST=A
SW
X/X+
B/B+
A
SW
UPDATE
Z
Zd
C
U
STATE REG SW COND BITS
42
MUX
MUX
41
ALU
ALU CODE
43
MEMORY WRITE
MUX/SP
15
ADR OF REQ
WORD 16 BIT
HIGH BYTE
LOW BYTE
DUAL PORT MEMORY

FIG. 17


K=0040
A
43
AND
ALU
Z
Z-1
C
U
Z=1 IF THE BIT OF A SELECTED IS "0"
K=8000
B
AND
ALU
43
Zd
BCRC
POLYGEN
XOR
ALU
43
STATE MODIFICATION
RESULT